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SCHEDULE

Part A

Hardware Binaries:

FPGA bitstream file for any or all of the Hardware Source identified below in this Part A

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Software Binaries:

Motherboard configuration controller Daughterboard configuration controller Daughterboard Application note SelfTest SCP firmware

Documentation:

Documentation, provided as PDF

Hardware Source

Hardware netlists of the ARM CoreLink peripheral technology and components known as TLX-400, NIC-400, and PL330

Part B

Wrapper:

Application Note wrapper file provided as hardware source files and netlists.

Part C: Example Code

- (i) Platform specific libraries and source code.
- (ii) ARM source code of Application note SelfTest.

Part D: Separate Files

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/end

ARM contract references: LES-PRE-20435 JUNO ARM DEVELOPMENT PLATFORM DELIVERABLES